

HYBRID ACTIVE MATRIX
THIN-FILM TRANSISTOR DISPLAY

Related Applications

- [0001] This application is related to commonly-assigned, co-pending:
- [0002] US Patent Application Serial No. 10/102,472, entitled "Pixel Structure for an Edge-Emitter Field-Emission Display," filed March 20, 2002, the contents of which are incorporated by reference herein.

Field Of The Invention

- [0003] This application is related to the field of vacuum displays and more specifically to flat panel displays using Thin Film Transistor (TFT) technology.

Background Of The Invention

[0004] Flat panel display (FPD) technology is one of the fastest growing technologies in the world with a potential to surpass and replace Cathode Ray Tubes (CRTs) in the foreseeable future. As a result of this growth, a large variety of the FPDs, ranging from very small virtual reality eye tools to large TV-on-the-wall displays, will soon become available. Thin displays will operate with digital signal processing that affords high-definition screen resolution.

[0005] Some of the more important requirements of FPDs are video rate of the signal processing; resolution typically above 100 DPI (dots per inch); color; contrast ratios greater than 20; flat panel geometry; screen brightness above 100 candles/meter squared (cd/m^2); and large viewing angle.

[0006] At present, liquid crystal displays (LCD) dominate the FPD market. However, although significant technological progress has been made in recent years, LCDs still have some drawbacks and limitations that pose considerable restraints. First, LCD technology is rather complex, which results in a high manufacturing cost and price of the product. Other

deficiencies, such as small viewing angle, low brightness and relatively narrow temperature range of operation, make application of the LCDs difficult in many high market value areas such as car navigation devices, car computers, and mini-displays for cellular phones.

[0007] Other FPD technologies capable of competing with the LCDs are currently under investigation. Among these technologies, plasma displays and field-emission displays (FED) are considered to be the most promising. Plasma displays employ a plasma discharge in each pixel to produce light. One limitation associated with plasma displays is that the pixel cells for plasma discharge cannot be made very small without affecting neighboring pixel cells. This is why the resolution in plasma FPD is poor for small format displays and becomes more efficient as the display size increases above 30" diagonally. Another limitation associated with plasma displays is that they tend to be thick as compared to FPDs. A typical plasma display has a thickness of about 4 inches.

[0008] Field Emission Displays (FEDs), on the other hand, employ "cold cathodes" which produce mini-electron beams that activate phosphor layers in the pixel. It has been predicted that FEDs will replace LCDs in the future. Currently, many companies are involved in FED development. However, after ten years of effort FEDs are not yet in the market.

[0009] FED mass production has been delayed for several reasons. One of these reasons concerns the fabrication of the electron emitters. The traditional emitter fabrication is based on forming multiple metal (Molybdenum) tips, see C.A. Spindt "Thin-film Field Emission Cathode," Journal. Of Appl. Phys., v. 39, 3504, and U.S. Patent 3,755,704 issued to C.A. Spindt. The metal tips concentrate an electric field, activating a field-induced auto-electron emission to a positively biased anode. The anode contains light emitting phosphors which produce an image when struck by an emitted electron. The technology for fabricating the metal tips, together with

necessary controlling gates, is rather complex. This fabrication process requires a sub-micron, electron-beam lithography and angled metal deposition in a large base electron-beam evaporator.

[00010] Another difficulty associated with FED mass production relates to the lifetime of FEDs. Electrons striking the phosphors result in phosphor molecule dissociation and formation of gases, such as sulfur oxide and oxygen, in the vacuum chamber. The gas molecules reaching the tips cloud or shield the electric field resulting in a reduction of the efficiency of electron emission from the tips. A second group of gases, produced by electron bombardment, contaminates the phosphor surface and forms undesirable energy band bending at the phosphor surface. This prevents electron-hole diffusion from the surface into the depth of the phosphor grain resulting in a reduction of the light radiation component of electron-hole recombination from the phosphor. These gas formation processes are interrelated and directly connected with vacuum degradation in the display chamber.

[00011] The gas formation processes are most active in the intermediate anode voltage range of 200-1000V. If, however, the voltage is elevated to 6-10kV, the incoming electrons penetrate deeply into the phosphor grain. In this case, the products of phosphor dissociation are sealed inside the grain and cannot escape into the vacuum. This significantly increases the life time of the FED and makes it close to that of a conventional cathode ray tube.

[00012] The high anode voltage approach is currently accepted by all FED developers. This, however, creates another problem. To apply such a high voltage, the anode must be made on a separate substrate and removed from the emitter a significant distance equaling about 1mm. Under these conditions, the gate controlling efficiency decreases, and pixel cross-talk becomes a noticeable factor. To prevent this effect, an additional electron beam focusing grid is introduced between the first grid and the anode, see, e.g., C.J. Spindt, et al., "Thin CRT Flat-Panel-Display

Construction and Operating Characteristics," SID-98 Digest, p. 99, which further complicates display fabrication.

[00013] Some existing tip-based FEDs include an additional electron beam focusing grid. Such FEDs include an anode, a cathode having a plurality of metal tip-like emitters, and a control gate made as a film with small holes above the tips of the emitters. The emitter tips produce mini-electron beams that activate phosphors coated on the anode. The phosphors are coated with a thin film of aluminum. The metal tip-like emitters and holes in the controlling gate, which are less than 1 μm in diameter, are expensive and time consuming to manufacture, hence they are not readily suited for mass production.

[00014] Another approach to FED emitter fabrication involves forming the emitter in the shape of a sharp edge to concentrate the electric field. See U.S. Patent 5,214,347 entitled "Layered Thin-Edge Field Emitter Device" issued to H.F. Gray. The emitter described in this patent is a three-terminal device for operation at 200V and above. The emitter employs a metal film, the edge of which operates as an emitter. The anode electrode is fabricated on the same substrate, and is oriented normally to the substrate plane, making it unsuitable for display functions. A remote anode electrode is provided parallel to the substrate, making it suitable for display purposes. The anode electrode, however, requires a second plate which significantly complicates the fabrication of the display.

[00015] Still another approach to FED emitter fabrication can be found in U.S. Patent 5,345,141, entitled "Single Substrate Vacuum Fluorescent Display," issued to C.D. Moyer, et al., which relates to the edge-emitting FED. The pixel structures described in U.S. Patent 5,345,141 include a diamond film deposited on top of a metal film and only the diamond edge is exposed.

Thus, only a relatively small fringing electric field coming from the metal film underneath the diamond film contributes to the field emission process.

[00016] Another limitation of FEDs is that the emitter films, including the diamond film and the insulator film, are grown on a phosphor film. The phosphor film is known to have a very rough surface morphology that makes it unsuitable for any further film deposition.

[00017] A pixel structure that reduces some of the noted problems with current FED technology is disclosed in commonly-assigned, co-pending, US Patent Application Serial No. 10/102,472, entitled "Pixel Structure for an Edge-Emitter Field-Emission Display," filed March 20, 2002. This application depicts an FED pixel that eliminates emitter tips in the FED cathode. In this application, electrons are emitted from the edges of electron emitting materials, such as alpha-carbon.

[00018] Although the pixel structure disclosed in the above-noted co-pending application reduces some of the problems, there is a need for a FED pixel design which substantially eliminates the problems associated with FED fabrication and allows for mass production of same.

Summary of the Invention

[00019] A cold-cathode vacuum flat panel display using thin-film-transistor (TFT) circuit is disclosed. Associated with each pixel element is a TFT circuit comprising a first and second active devices electrically cascaded and a capacitor in communication with an output of the first device and an output of the second device that may be used to selectively address pixel elements in the display. Cold cathode sources are used to emit electrons that are drawn to selected pixel elements that include phosphor pads, which emit light of a known wavelength when struck by the emitted electrons.

Brief Description of the Drawings

[00020] Figure 1 illustrates a cross-sectional view of a TFT anode-based Field Emission Display (FED) in accordance with the principles of the invention;

[00021] Figure 2 illustrates a top view of a conventional embodiment of a TFT;

[00022] Figure 3 illustrates a circuit diagram of a conventional TFT circuit;

[00023] Figure 4 illustrates a cross-sectional view of a second embodiment of a TFT anode-based FED in accordance with the principles of the present invention;

[00024] Figure 5 illustrates a top view of an exemplary FED cathode in accordance with the principles of the present invention;

[00025] Figure 6 illustrates a cross-section view of another embodiment of the TFT based display shown in Figure 1 using an alternate cold cathode configuration;

[00026] Figure 7 illustrates a cross-sectional view of another embodiment of the TFT based display shown in Figure 4 using an alternate cold cathode configuration;

[00027] Figure 8 illustrates a cross-sectional view of another embodiment of a TFT-cold cathode based display;

[00028] Figure 9 illustrates a cross-sectional view of another embodiment of a TFT-cold cathode based display; and

[00029] Figure 10 illustrates a cross-sectional view of another embodiment of a TFT-cold cathode based display.

[00030] It is to be understood that these drawings are solely for purposes of illustrating the concepts of the invention and are not drawn to scale. The embodiments shown herein and described in the accompanying detailed description are to be used as illustrative embodiments and should not be construed as the only manner of practicing the invention. Also, the same

reference numerals, possibly supplemented with reference characters where appropriate, have been used to identify similar elements.

Detailed Description

[00031] Figure 1 illustrates a cross-sectional view of a TFT anode/cold cathode Field Emission Display (FED) element 100 in accordance with the principles of the present invention. In this exemplary embodiment, the display element 100 is composed of cathode 104 that acts as a low-voltage source of electrons, anode 106 that employs TFT technology to control the attraction of electrons 140 to corresponding pixel elements on the surface 160, and grid 150 between anode 106 and cathode 104 that serves to separate a negative potential on cathode 104 and a low positive voltage on the anode 106.

[00032] Cathode 104 is fabricated by progressively depositing onto substrate 110, conventionally a glass, an insulating material 115, a conductive material 117, an emitter material 120 operable to emit electrons, a second insulating layer 125, such as SiO₂, and a second conductive material 130. Emitter material 120 is selected from known materials that have a low work function for emitting electrons 140. Alpha-carbon is a well-known material for emitting electrons 140. The conductive material 117 beneath the emitter material 120 serves to reduce the resistance of the emitting layer and thus bring the emitter voltage to the edge 135 of emitter material 120. Wells 136 are then etched through the deposited second conductive layer 130, insulating layer 125, emitter layer 120, conductive layer 117 and insulating layer 115 using well-known photoetching methods. In this case, edges 135 of the emitter material 120 are exposed for the generation of electrons 140. Second conductive material 130 operates as a gate to draw electrons 140 from the edges 135 of emitter material 120 when a sufficient potential difference,

i.e., electron extraction voltage or threshold voltage, exists between conductive material 130 and conductive layer 117.

[00033] Anode 106 is composed of a plurality of conductive pads 170 fabricated in a matrix of substantially parallel rows and columns on surface 160 using known fabrication methods. In this illustrated embodiment surface 160 is a transparent surface such as glass. Conductive pads 170 are also composed of a transparent material, such as ITO (Indium Titanium Oxide).

[00034] A matrix organization, as will be shown in Figure 2, of conductive pads 170/phosphor layers 175 allows for known X-Y addressing of each of the conductive pads 170. In this case, conductive pad 170 may be representative of individual pixel elements in the display.

[00035] Deposited on each conductive pad 170 is phosphor layer 175. Phosphor layer 175, in one aspect of the invention, may be selected from materials that emit photons 195 of a specific color for a monochrome display. In a conventional RGB display, phosphor layer 175 may be selected from materials that produce a red light, green light or blue light 195 when struck by electrons 140. As would be appreciated by those skilled in the art, the terms "light" and "photon" are synonymous and are used interchangeably herein.

[00036] Associated with each conductive pad 170/phosphor layer 175 pixel element is a TFT circuit 180 that is operable to apply a known voltage to an associated conductive pad 170/phosphor layer 175 pixel element. TFT circuit 180 operates to apply either a first voltage to bias an associated pixel element to maintain it in an "off" state or a second voltage to bias an associated pixel element to maintain it in an "on" state, i.e., activate. In one embodiment, TFT circuit 180 may apply a zero voltage, $V_a=0$, to bias conductive pad 170 into an "off" state, or

apply a higher positive bias voltage, in the order of $V_a = 25\text{-}30$ volts, to bias conductive pad 170 into an "on" state. In this illustrated case, conductive pad 170 is inhibited from attracting electrons 140 emitted by cathode 104 when in an "off" state, and attract electrons 140 when in an "on" state.

[00037] The use of TFT circuitry 180 for biasing conductive pad 170 provides for the dual function of addressing pixel elements and maintaining the pixel element in a condition to attract electrons for a desired time period, i.e., time-frame or sub-periods of time-frame, as will be explained more fully with regard to Figures 2 and 3.

[00038] In the embodiment shown in Figure 1, grid 150 is interposed, relatively equidistant, between cathode 104 and anode 106. Grid 150, having a plurality of grid holes 152, smaller than the cathode-to-anode distance 190, creates an equi-potential line when a potential applied to grid 150 (V_g) is less than a potential applied to the anode (V_a) relative to the voltage applied to the cathode 104 (V_c). In one aspect, electrons 140 emitted by cathode 104 pass through grid 150 and impinge upon phosphor pad 175 when a corresponding conductive pad 170 is biased to an "on" state. Similarly, electrons are not attracted to the conductive pad 170 when a corresponding conductive pad 170 is biased to an "off" state.

[00039] Grid 150 further serves to separate the cathode 104 of a relatively high negative potential and a low voltage of TFT circuitry 180 for pixel control. It would be recognized by those skilled in the art that the role of a positively biased grid 150 is advantageous as it serves to unify the electron distribution in front of the phosphor pads. This operation is applicable when the electron energies are small and can be controlled by the potentials applied to the TFT circuitry. For example, when threshold voltage for extracting electrons is less than the TFT control voltage, i.e., anode voltage, grid 150 may not be necessary.

[00040] However, in another aspect, when the threshold (gate) voltage for electron extraction from emitter edge 135 is higher than a voltage applied to the anode, i.e., phosphor pads 170, via the TFT circuitry, the energies of electron 140 may be too high and not manageable by the relatively low TFT voltages. In this case, grid 150 may be used to decelerate the electrons approaching the phosphor pads by lowering the voltage applied to grid 150.

[00041] Although grid 150 is shown in this exemplary embodiment and has been discussed with regard to controlling emitted electrons, it would be recognized that the operation of display 100 is not dependent upon the presence of grid 150 and the embodiment shown in Figure 1 represents an exemplary embodiment of the invention.

[00042] The TFT FED 100 shown allows for a low voltage addressing on the anode and the use of inexpensive LCD drivers. Furthermore, the addressing circuit (not shown) on anode 106 eliminates the need for electron beam focusing methods necessary in conventional FED structures. The use of low voltage further eliminates problems of gas ionization and chamber breakdown characteristically associated with the use of high voltage FEDs. Furthermore, cathode 104 serves as a uniform electron source and provides for high screen brightness and uniformity. The separation of pixel control circuitry from cathode 104 is further advantageous as it makes the fabrication of the device simpler and increases the fabrication yield.

[00043] Figure 2 illustrates a top view of an example of a conventional TFT-based anode. In this illustrated example, anode 106 is organized in a matrix of electrically conductive rows, referred to as 210, and electrically conductive columns, referred to as 220. Associated with each row/column is an electrically conductive pad 170 and phosphor pad 175 that defines a pixel element.

[00044] Associated with each conductive pad 170/phosphor pad 175 and accessed by a row/column designation is TFT circuit 180. TFT circuit 180 operates to electrically disconnect an associated conductive pad 170/phosphor pad 175 when the associated pixel is intended to be in an “off” state and connect an associated conductive pad 170/phosphor pad 175 when it is intended to be in an “on” state. A known voltage, referred to as V_{dd} , is applied to each TFT circuit 180.

[00045] Figure 3 illustrates a circuit diagram of a conventional TFT circuit 180 associated with a single element in the matrix shown in Figure 2. TFT circuit 180 is composed of two transistor devices 182, 186, electrically cascaded, and capacitor 190 connected between the output of first device 182 and the output of second device 186. In the illustrated embodiment, devices 182, 186 are FETs (Field Effect Transistors). FETs are known in the art to possess a high input impedance.

[00046] In the illustrated embodiment, gate node 183 of FET 182 is electrically connected to and associated with row line 210, and node 184 of FET 182 is associated with column line 220. The output node 185 of FET 182 is electrically cascaded to gate electrode 187 of FET 186, and to capacitor 190.

[00047] Electrode 188 of FET 186 is electrically connected to constant voltage source, typically V_{dd} , and output electrode 189 is electrically connected to electrically conductive pad 170. Capacitor 190 is also further connected between the gate and the source node of FET 186.

[00048] In operation, when FET 182 is in an “on” state, by the application of a voltage on row line 210, a voltage applied to column line 220 is passed through FET 182 and concurrently present at, or applied to, gate node 187 of FET 186 and capacitor 190. Capacitor 190 is charged to substantially the same voltage value as applied to column 220. When voltage on row line 210

is removed, capacitor 190 operates to substantially maintain the same potential as is on column line 220 to gate electrode 187. This voltage is maintained for a known period of time, which is based on the value of capacitor 190 and an impedance of FET 182. Capacitor 190 thus operates to substantially “hold” the voltage even after the voltage or potential to selected row 210 is removed.

[00049] As voltage or potential is applied to gate terminal 187 of FET 186, FET 186 is in an “on” state and the constant, fixed voltage or potential, V_{dd} , applied to node 188, which is also referred to as an anode voltage (V_a), is passed through FET 186 to node 189 and associated pad 170. Pad 170 then is operable to attract electrons 140 (not shown) drawn from cathode 104. When the gate electrode 187 voltage is removed, the corresponding pixel is switched to an “off” state as the potential at electrode 189 is relatively low, i.e., near zero volts. In one aspect of the invention, the anode voltage may be in the range of about 20-30 volts.

[00050] Thus, TFT circuit 180 provides for both “pixel selection” and “pixel hold” functions. Accordingly, electrons 140 may continue to be attracted to the corresponding conductive layer 170 for a desired time frame without the concurrent application of a voltage on a corresponding row line.

[00051] Capacitor 190 is sized to be commensurate with the desired frame time and the input impedance of the second active device 186. The value of capacitor 190 may be selected such that the decay of the stored charge through the impedance of first device 182 is in the order of or larger than the desired frame time.

[00052] Returning to Figure 2, although the exemplary display matrix has been described as a monochromatic display having six pixel elements, those skilled in the art should readily recognize that Figure 2 may also represent a color display having three color pixels with each

color pixel having associated red, green and blue phosphor layers. While the present color display is described with the use of conventional RGB (red, green, blue) technology, the use of phosphor layers that emit light of alternate colors, visible and non-visible, is considered within the scope of the invention.

[00053] Figure 4 illustrates a second embodiment of the display. In this embodiment, the TFT anode structure shown in Figure 2 is deposited on substrate 110. In this case, a material such as poly-silicon or amorphous silicon, may be deposited on substrate 110, that allows for the fabrication of row lines 210 (not shown), column lines 220 (not shown), conductive pad 170 and TFT circuit 180 onto substrate 110 in row/column matrix as shown in Figure 2. Phosphor layer 175 may then be deposited on corresponding conductive pads 170.

[00054] In one aspect a silicon (Si) single crystal wafer may be used for the active matrix circuitry, wherein the Si wafer is attached to a glass substrate. In this case, the phosphor pads are also made on the Si wafer.

[00055] Cathode 104 is fabricated on viewing surface 160 and emitter layer 120 and conductive layer 130 operate to draw electrons from edges 135 of emitter layer 120. Emitter layer 120 and conductive layer 130 occupy a significantly small portion of the viewing glass area to allow for photons to be viewed through cathode 104 and transparent viewing glass 160. As would be appreciated, elements of cathode 104 may be composed of optically transparent materials.

[00056] As in the embodiment shown in Figure 1, grid 150 may have a dual function in both unifying the electron distribution approaching the phosphor pads and decelerating the electron. This latter function may be needed when the threshold voltage for electron extraction from the emitter edge is too high to be controlled by the voltages on the TFT circuit.

[00057] Figure 5 illustrates a top view of an exemplary cathode 104 in accordance with the principles of the invention. It is desired that cathode 104 serves as a uniform electron source when the voltage applied to conductive layer 130 is sufficiently positive relative to emitter layer 120. In this exemplary embodiment, wells 136 are formed within the conductive layer 130 as elongated slots 510, which increase the length of emitter edges 135 (not shown). Increased emitter edge 135 length provides for an increased edge area for the emission of electrons 140.

[00058] In this exemplary view, wells 136 are etched through conductive layer 130 to expose the emitter layer edges. Edges 135 (not shown) of emitter layer 120 are formed beneath edges 137 of conductive layer 130.

[00059] Figure 6 illustrates another exemplary embodiment of a TFT based display 600 wherein cathode 104a is composed of a plurality of carbon nanotubes 610 placed on conductive material 615 located within well 136. In this case, conductive layer 130, electrically isolated from material 615, operates as a gate that may be used to draw electrons 140 from nanotubes 610, when the potential difference between gate 130 and nanotube 610 exceeds a threshold for electron extraction. Nanotubes 610 are known to possess extremely low threshold voltages in the order of 1-3 V/micron for electron emission. Cataphoretic deposition or printing of nanotubes 610 on a metal surface is known in the art.

[00060] Similar to the design shown in Figure 1, grid 150 is also shown in this exemplary embodiment to control and decelerate, if necessary, the flow of electrons 140 directed toward phosphor layer 175. Anode 106 is similar to that described with regard to Figure 1 and its description need not be repeated.

[00061] Figure 7 illustrates another exemplary embodiment of a TFT-cold cathode based display 700, wherein cathode 104b is composed of a plurality of carbon nanotubes 610 that are

uniformly distributed on a conductive layer 710 on substrate 110. Grid 150 is also shown in this embodiment and is used for extracting electrons 140 emitted by nanotubes 610 and directed toward phosphor layer 175. In this embodiment, second grid 155 is included to decelerate electrons so that they are controllable by the TFT circuitry. Anode 106 is similar to that described with regard to Figure 1 and its description need not be repeated.

[00062] Figure 8 illustrates an embodiment of a TFT-cold cathode based display 800 constructed similar to the display shown in Figure 1, i.e., anode on viewing surface. In this embodiment, cathode 104d is composed of nanotubes 610 deposited on cathode filament 805. In this case, electrons 140 are emitted from nanotubes 610 when a voltage difference between grid 150 and cathode filament 805 is sufficient to extract electrons 140. Grid 150 is located in the range of 100-200 microns above substrate 110. Second grid 810, which is used to decelerate electrons 140, is located between grid 150 and anode 106. Anode 106 is similar to that described with regard to Figure 1 and its description need not be repeated.

[00063] Figure 9 illustrates another exemplary embodiment of a TFT-cold cathode based display 900 constructed similar to the display shown in Figure 4, i.e., anode on back surface. In this embodiment, cathode 104d is composed of nanotubes 610 on cathode filament 805 as previously described, and grids 150 and 810 are installed between nanotubes 610 and anode 106, to control and decelerate the flow of electrons to anode 106. Anode 106 is similar to that described with regard to Figure 4 and its description need not be repeated.

[00064] Figure 10 illustrates an embodiment of a TFT-cold cathode based display 1000 constructed similar to the display shown in Figure 4, i.e., anode on back surface. In this case, cathode 104f is composed of nanotubes 610 on a transparent conductive layer 1010. Grids 150 and 810 are installed between cathode 104f and anode 106 to extract and control the flow of

electrons 140 to anode 106. Grid 810 is used to decelerate the flow of electrons when the electron energies are too high to be controlled by the low anode voltage of the TFT circuit 180. Anode 106 is similar to that described with regard to Figure 4 and its description need not be repeated.

[00065] Although not shown or discussed in detail, it would be understood by those skilled in the art that insulating spacers may be distributed throughout the display to electrically isolate the electrical potential applied to the elements disclosed, to separate two plates from each other and to sustain the evacuated pressure. It should be further understood that the spacers may be used to reduce glass plate thickness and thus decrease both weight and thickness of the display. It should also be understood that the edges of the overall display may be sealed and that the space between the cathode and the anode may be evacuated to a level of at least 10^{-5} tor.

[00066] While there has been shown, described, and pointed out fundamental novel features of the present invention as applied to preferred embodiments thereof, it will be understood that various omissions and substitutions and changes in the apparatus described, in the form and details of the devices disclosed, and in their operation, may be made by those skilled in the art without departing from the spirit of the present invention. It is expressly intended that all combinations of those elements that perform substantially the same function in substantially the same way to achieve the same results are within the scope of the invention. Substitutions of elements from one described embodiment to another are also fully intended and contemplated.